REMARKS

Claims 6-8, 10-19, 22-24, 27-28 have been amended.

Claims 6, 7, 27, and 28 have been amended cosmetically to make the subject matter clearer. In particular, structure style language in the preamble of these claims has been changed to method style language. No new matter has been added.

Claims 6-28 are pending.

In view of the above amendments and the following remarks, the applicants respectfully request withdrawal of each of the rejections and allowance of the application.

Applicant's remarks, below, are preceded by quotations of the related comments of the Examiner, in small, bold-face type.

Specification

2. Claim 27 is objected to because of the following informalities: 2nd paragraph second line part of the sentence reads "layer continuing". Appropriate correction is required.

Claim 27 has been amended to clarify the subject matter. In particular, the word "continuing" in claim 27 has been changed to "continuous with." Support for such a change can be found, for example, in FIG. 5b and on page 12, lines 5-24 of the application.

In view of the above corrections and remarks, the applicants respectfully request the withdrawal of the request for correction.

Claim Rejections – 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 6, is rejected under 35 U.S.C. 102(b) as being anticipated by Hsing et al., US patent No. 5,517,046.

Regarding claim 6, Hsing teaches a method f manufacturing a semiconductor device provided with high concentration source/drain layers 32 and 34 respectively of the reverse conductive type formed in a semiconductor layer 20 of one conductive type, a gate electrode 26 formed on a channel layer located between the source and drain layers, a body layer 29 of one conductive type formed in the vicinity of the source layer and a low concentration drain layer 31 of the reverse conductive type formed between the channel layer and the drain layer, wherein the step of forming a body layer of one conductive type comprises a step of doping impurities of one conductive type into the semiconductor layer by ion implantation (fig. 3 and column 3, lines 7-62).

Regarding claims 7 and 16, Hsing teaches the entire claimed process of claim 6 above including the above process comprising the steps of doping impurities of the reverse conductive type into the semiconductor layer to form a low concentration drain layer 31 of the reverse conductive type; doping impurities of the reverse conductive type into the semiconductor layer to form a high concentration source layer 32 of the reverse conductive type so that the source layer is adjacent to one end of the gate electrode 26 and form a high concentration drain layer 34 of the reverse conductive type in a position apart from the other end of the gate electrode; doping impurities of one conductive type into the semiconductor layer to form a body layer 29 of one conductive type extended from under one end of the gate electrode and formed so that the body layer is adjacent to the source layer 32 of the reverse conductive type; and forming a gate electrode 26 on a gate oxide film 24 after the gate oxide film is formed on the semiconductor layer (fig. 3 and column 3, lines 7-62).

Regarding claim 8, Hsing teaches the entire claimed process of claim 7 above including the step of doping an impurity for forming a reverse conduction type layer by ion implantation (fig. 3 and column 3, lines 38-39).

Amended independent claim 6 recites a method of manufacturing a semiconductor device that includes a gate electrode and:

> forming a body layer of one conductive type adjacent to the source layer and a low concentration drain layer of the reverse conductive type formed between the channel layer and the drain layer, wherein the body layer is formed only under the gate electrode

Support for such an amendment can be found, for example, in FIGS. 10 and 12 and on page 18, lines 6-19 of the application. Such a structure has certain advantages as discussed, for example, on page 4, line 17 to page 5, line 20 of the application. The body layer formed under the gate electrode has advantages, such as a reduction in junction capacitance or no need of high temperature for forming the body layer, among others.

Hsing discloses a semiconductor device that includes a body layer 29 that **extends** from under a gate electrode 26 and covers a high concentration source layer 32. (see FIG. 3) In

contrast, in the present invention, the body layer does **not** extend beyond the gate electrode, instead "the body layer is formed **only under** the gate electrode" as recited in claim 6.

Moreover, in Hsing, the body layer 29 is **separate** from the drain layer 31 and not **adjacent** to the drain layer 31. In contrast, in the present invention, the device includes "a body layer of one conductive type **adjacent** to the source layer **and** a low concentration drain layer" as recited in claim 6. Thus, Hsing does not disclose, teach or suggest claim 6.

Independent claim 7 recites a method that includes the limitation recited in claim 6 as explained above. Since claim 6 should be allowable for the reasons explained above, claim 7 should also be allowable for at least the same reasons. Since claims 8 and 16 depend on claim 7, claims 8 and 16 should be allowable for at least the same reasons as claim 7.

In light of the above amendments and remarks, the applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection of claims 6, 7, 8 and 16.

Claims 22-26, are rejected under 35 U.S.C. 102(b) as being anticipated by Pfiester et al., US patent No. 4,948,745.

Regarding claim 22, Pfiester teaches a method of manufacturing a semiconductor device comprising source/drain regions 65 and 66 of a second conductive type in a semiconductor of a first conductive type 54 and a semiconductor layer of a first conductive type constituting a channel 76 located between the source/drain regions of the second conductive type, the method comprising: doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form the semiconductor layer of the first conductive type (fig. 7).

Regarding claim 23, Pfiester teaches 23 a method of manufacturing a semiconductor device comprising low concentration source/drain regions 63 and 64 of a second conductive type in a semiconductor of a first conductive type 54, high concentration source/drain regions 65 and 66 of the second conductive type in the low concentration source/drain regions and a semiconductor layer of the first conductive type constituting a channel 76 located between the source/drain regions of the second conductive type, the method comprising: doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form the semiconductor layer of the first conductive type (fig. 7).

Regarding claim 24, Pfiester teaches the entire claimed process of claim 23 above including doping impurities of a second conductive type into a semiconductor of a first conductive type to form low concentration source/drain regions of the second conductive type; doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer; and forming a gate electrode 70 on a gate oxide film 62 pr vided on the semiconductor of the first conductive type (fig. 7).

Regarding claims 25 and 26, Pfiester teaches the entire claimed process f claim 24 above including the low concentration source/drain regions of the second conductive type are formed to be adjacent to the semiconductor layer of the first conductive type formed below the gate electrode by ion implantation (fig. 7).

Independent claim 22 recites a method that includes:

forming source/drain regions of a second conductive type in a semiconductor of a first conductive type;

doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form a semiconductor layer of the first conductive type comprising a channel located between the source/drain regions; and

doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer.

Support for such an amendment can be found, for example, on page 21, lines 1-25 of the application.

The Office Action (page 4, second paragraph) states that Pfiester teaches a semiconductor layer of a first conductive type constituting a channel (Fig. 7). However, Pfiester does not teach or suggest "doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer" as recited in claim 22. Moreover, the Hsing and Pfiester references fail to disclose or suggest, alone or in combination, such a limitation. Therefore, claim 22 is patentably distinct over the cited references.

Independent claim 23 recites a method that includes a limitation similar to claim 22. Since claim 22 is patentable for the reasons above, claim 23 should be allowable for at least the same reasons as claim 22.

Independent claim 24 recites a method that includes:

doping impurities of the second conductive type into the semiconductor of the first conductive type to form high concentration source/drain regions of the second conductive

type in the low concentration source/drain regions, wherein the low concentration source/drain regions surround the high concentration source/drain regions;

forming a gate electrode on a gate oxide film provided on the semiconductor of the first conductive type, wherein the low concentration source/drain regions extend from under the gate electrode.

Support for such an amendment can be found, for example, in FIGS. 10 and 12 and on page 18, lines 6-19 of the application. Such a structure has certain advantages as discussed on page 10 of the present response.

Pfiester discloses a method for fabricating semiconductor devices that includes lightly doped source/drain regions 63, 64, and highly doped source/drain regions 65, 66. (see FIG. 7) The lightly doped regions 63, 64 are **adjacent** to the highly doped regions 65, 66. In contrast, in the present invention, the "low concentration source/drain regions **surround** the high concentration source/drain region" as recited in claim 24.

Moreover, in Pfiester, the lightly doped regions 63, 64 are aligned with a region 70. (see FIG. 7 and column 6, lines 16-20). The lightly doped regions 63, 64 do **not** extend below the region 70, whereas, in the present invention, the "low concentration source/drain regions **extend** from under the gate electrode" as recited in claim 24. Such a structure has certain advantages as discussed on page 10 of the present response. Thus, Pfiester does not disclose, teach or suggest claim 24.

Since claims 25 and 26 depend on claim 24, claims 25 and 26 should be allowable for at least the same reasons as claim 24.

In light of the above amendments and remarks, the applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection of claims 22-26.

Claim Rejections – 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior**

art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9, is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing in view of Chen et al. US patent No. 5,926,712.

Regarding claim 9, Hsing teaches substantially the entire claimed process of claim 7 above except explicitly stating that the low concentration drain layer of the reverse conductive type or the low concentration source/drain layers of the reverse conductive type are formed so that they are shallow under said gate electrode and they are deep under the high concentration drain layer of the reverse conductive type or the high concentration source/drain layers of the reverse conductive type.

It is conventional and also taught by Chen forming a low concentration drain layer 216 that is shallow under the gate and deeper under the high concentration drain region as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made incorporate the low concentration drain layer taught by Chen in the method of Hsing.

Claim 9 is patentable over Hsing in view of Chen for the reasons given below.

Hsing discloses a semiconductor device that includes a body layer 29 that **extends** from under a gate electrode 26 and covers a high concentration source layer 32. (see FIG. 3) In contrast, in the present invention, the body layer does **not** extend beyond the gate electrode, instead "the body layer is formed **only under** the gate electrode" as recited in claim 7.

Moreover, in Hsing, the body layer 29 is **separate** from the drain layer 31 and not **adjacent** to the drain layer 31. In contrast, in the present invention, the device includes "a body layer of one conductive type **adjacent** to the source layer **and** a low concentration drain layer" as recited in claim 6. Thus, Hsing does not disclose, teach or suggest claim 7.

Since claim 9 depends from claim 7, claim 9 should be allowable for at least the same reasons as claim 7.

In light of the above remarks, the applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claim 9.

Claims 10-15, 17, 18, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Hsing.

Regarding claims 10 and 17, Chen teaches a method of manufacturing a semiconductor device, comprising the steps of doping impurities f the reverse c nductive type into a semiconductor layer of one conductive type to form low concentration source/drain layers 216 of the reverse conductive type; doping impurities of the reverse conductive type into the semiconductor layer and forming a layer of the reverse conductive type into the semiconductor layer and forming a layer of the reverse conductive type which ranges to the source/drain layers of the reverse conductive type and is shallower than the source/drain layers of the reverse conductive type; doping impurities of the reverse conductive type into the source/drain layers of the reverse conductive type to form high concentration source/drain layers 219 of the reverse conductive type; and forming a gate electrode 215 on a gate oxide film so that the gate electrode covers said body layer of one conductive type after the gate oxide film 214 is formed on the substrate.

Chen does not teach doping impurities of one conductive type into the layer of the reverse conductive type to form a body layer of one conductive type.

It is conventional and also taught by Hsing to form a body layer 29 by doping impurities of one conductive type as claimed using ion implantation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the body layer taught by Hsing in the method of Chen in order to improve breakdown voltage.

Regarding claims 11-15, 18 and 19, the combined teaching of Chen and Hsing teaches substantially the entire claimed process of claim 10 above including doping an impurity for forming a reverse conduction type layer by ion implantation after forming the body layer, forming a first gate electrode for a first MOS transistor on a gate oxide film after the gate oxide film is formed on the substrate and forming a second gate electrode 26 for a second MOS transistor on the body layer 29 of one conductive type; and forming source/drain layers of the reverse conductive type so that they are adjacent to the first gate electrode using a resist film coating an area except are as where source/drain layers for the first MOS transistor are formed as a mask (Chen, fig. 2 column 3, lines 35-67 and column 4, lines 1-31 and Hsing, fig. 3 and column 3, lines 38-39).

The limitation using a resist film coating an area is not taught by the combined teaching of Chen and Hsing.

The use of photolithographic process is a well-known process that is commonly used in the fabrication of semiconductor devices.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use conventional photolithographic technique for precise patterning of layers.

Regarding claim 20 and 21, the combined teaching of Chen and Hsing teaches substantially the entire claimed process of claims 12 and 14 above the first MOS transistor is a micro MOS transistor; and the second MOS t4ansistor is a MOS transistor having high resistance to voltage.

The limitation that the above transistor is a micro MOS is conventional device that is commonly fabricated in semiconductor fabrication.

With regards to the limitation that the MOS transistor having a high resistance to voltage, this characteristic is considered to be inherent characteristic f most transist rs since any layer have a resistance to voltage value.

Independent claim 10 recites a method of manufacturing a semiconductor device that includes:

> forming a gate electrode on a gate oxide film so that the gate electrode covers said body layer of one conductive type after the gate oxide film is formed on said substrate, wherein the body layer is formed only under the gate electrode.

Support for such an amendment can be found, for example, in FIGS. 10 and 12 and in page 18, lines 6-19 of the application. Such a structure has certain advantages as discussed on page 10 of the present response.

Chen discloses a process for fabricating a semiconductor device that includes low concentration source/drain layers 216, high concentration source/drain layers 219 formed on layers 216, and a gate electrode 215. (see FIGS. 2(a) to 2(f)) Hsing discloses a body layer 29 that **extends** from a gate electrode 26 to cover a high concentration source layer 32. (see FIG. 3) In contrast, in the present invention, "the body layer is formed **only under the gate electrode**" as recited in claim 10. Such a structure in the present invention provides various advantages as referenced above. Moreover, the fact that in Hsing the body layer 29 **extends** beyond the gate electrode that teaches away from the claim invention wherein the body layer is formed **only under the gate electrode**. Thus, the above references, alone or in combination, fail to disclose, teach or suggest claim 10.

Since claim 11 depends on claim 10, claim 11 should be allowable for at least the same reasons as claim 10.

Independent claim 12 recites a method that includes a limitation similar to the above limitation in claim 10. Since claim 10 should be allowable for the reasons explained above, claim 12 should also be allowable for at least the same reasons. Since claims 13, 17, 18 and 20 depend on claim 12, claims 13, 17, 18, and 20 should be allowable for at least the same reasons.

Likewise, independent claim 14 recites a method that includes a limitation similar to the above limitation in claim 10. Since claim 10 should be allowable for the reasons explained above, claim 14 should also be allowable for at least the same reasons. Since claims 15, 19, and 21 depend on claim 14, claims 15, 19, and 21 should be allowable for at least the same reasons.

In light of the above amendments and remarks, the applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claims 10-15, 17, 18, 19, and 21.

Regarding claims 27 and 28, Pfiester teaches substantially the entire claimed process of claim 24 above except explicitly stating suing a resist film, as a mask, having an opening in a region for forming the second transistor to form a low concentration second conductive type layer connecting the second low concentration source/drain regions; and doping impurities of the first conductive type by using a resist film, as a mask.

The use of photolithographic process is a well-known process that is commonly used in the fabrication of semiconductor devices.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use conventional photolithographic technique for precise patterning of the layers.

The limitation the semiconductor device comprising a first transistor having high resistance to voltage and a second transistor having high resistance to voltage is not taught Pfiester explicitly.

The claimed characteristic is considered to be inherent characteristic of most transistors since any layer have a resistance to voltage value. Therefore layers 76 and 92 have inherent resistance to voltage value.

Claim 27 recites a method that includes low concentration source/drain regions and a gate electrode, wherein:

> the low concentration source/drain regions extend from under the gate electrode, and the low concentration source/drain regions surround the high concentration source/drain regions

Support for such an amendment can be found, for example, in FIGS. 10 and 12 and in page 18, lines 6-19 of the application. Such a structure has certain advantages as discussed on page 10 of the present response.

As mentioned above (see 102(b) rejection of claims 22-26), the Pfiester reference does not disclose, teach or suggest claims 22-26. Independent claim 27 recites a method that includes a limitation similar to the above limitation in claim 22. Since claim 22 should be allowable for the reasons explained above, claim 27 should also be allowable for at least the same reasons.

Likewise, independent claim 28 has been amended to recite a method that includes a limitation similar to the above limitation in claim 22 (or 27). Since claim 22 (or 27) should be allowable for the reasons explained above, claim 28 should also be allowable for at least the same reasons.

In light of the above amendments and remarks, the applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claims 27 and 28.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 9/4/02

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Version with markings to show changes made

In the claims:

Claims 6-8, 10-19, 22-24, and 27-28 have been amended as follows:

--6. (Amended) A method of manufacturing a semiconductor device [provided with] comprising:

forming high concentration source/drain layers of the reverse conductive type [formed] in a semiconductor layer of one conductive type[,];

forming a gate electrode [formed] on a channel layer located between the source and drain layers[,]; and

forming a body layer of one conductive type [formed in the vicinity of] adjacent to the source layer and a low concentration drain layer of the reverse conductive type formed between the channel layer and the drain layer, wherein the body layer is formed only under the gate electrode, and wherein [the step of] forming a body layer of one conductive type comprises [a step of] doping impurities of one conductive type into said semiconductor layer by ion implantation.--

--7. (Amended) A method of manufacturing a semiconductor device [provided with high] comprising:

forming concentration source/drain layers of the reverse conductive type [formed] in a semiconductor layer of one conductive type[,];

forming a gate electrode formed on a channel layer located between the source and drain layers[,];

forming a body layer of one conductive type formed [in the vicinity of] adjacent to the source layer and a low concentration drain layer of the reverse conductive type formed between the channel layer and the drain layer, wherein the body layer is formed only under the gate electrode; [,comprising the steps of:]

doping impurities of the reverse conductive type into said semiconductor layer to form a low concentration drain layer of the reverse conductive type;

doping impurities of the reverse conductive type into said semiconductor layer to form a high concentration source layer of the reverse conductive type so that the source layer is adjacent to one end of said gate electrode and form a high concentration drain layer of the reverse conductive type in a position apart from the other end of said gate electrode;

doping impurities of one conductive type into said semiconductor layer to form a body layer of one conductive type extended from under one end of said gate electrode and formed so that the body layer is adjacent to said source layer of the reverse conductive type; and

forming a gate electrode on a gate oxide film after the gate oxide film is formed on said semiconductor layer.--

--8. (Amended) A method of manufacturing a semiconductor device according to claim 7, further comprising [a step of] doping an impurity for forming a reverse conduction type layer by ion implantation.--

--10. (Amended) A method of manufacturing a semiconductor device, comprising [the steps of]:

doping impurities of the reverse conductive type into a semiconductor layer of one conductive type to form low concentration source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said semiconductor layer and forming a layer of the reverse conductive type which ranges to said source/drain layers of the reverse conductive type and is shallower than said source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said source/drain layers of the reverse conductive type to form high concentration source/drain layers of the reverse conductive type;

doping impurities of one conductive type into said layer of the reverse conductive type to form a body layer of one conductive type; and

forming a gate electrode on a gate oxide film so that the gate electrode covers said body layer of one conductive type after the gate oxide film is formed on said substrate, wherein the body layer is formed only under the gate electrode.--

--11. (Amended) A method of manufacturing a semiconductor device according to Claim 10, further comprising [a step of] doping an impurity for forming a reverse conduction type layer by ion implantation after forming the body layer.--

--12. (Amended) A method of manufacturing a semiconductor device, comprising [the steps of]:

doping impurities of the reverse conductive type into a semiconductor layer of one conductive type to form a low concentration layer of the reverse conductive type;

doping impurities of the reverse conductive type into said layer of the reverse conductive type to form high concentration source/drain layers of the reverse conductive type;

doping impurities of one conductive type into said layer of the reverse conductive type to form a body layer of one conductive type;

forming a first gate electrode for a first MOS transistor on a gate oxide film after the gate oxide film is formed on said substrate and forming a second gate electrode for a second MOS transistor on said body layer of one conductive type, wherein the body layer is formed only under the gate electrode; and

forming source/drain layers of the reverse conductive type so that they are adjacent to said first gate electrode using a resist film coating an area except are as where source/drain layers for said first MOS transistor are formed as a mask.--

--13. (Amended) A method of manufacturing a semiconductor device according to Claim 12, further comprising [a step of] doping an impurity for forming a reverse conduction type layer by ion implantation.--

--14. (Amended) A method of manufacturing a semiconductor device, comprising [the steps of]:

doping impurities of the reverse conductive type into a semiconductor layer of one conductive type by ion implantation to form low concentration source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said semiconductor layer by ion implantation to form a layer of the reverse conductive type which ranges to said source/drain layers of the reverse conductive type and is shallower than said source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said source/drain layers of the reverse conductive type by ion implantation to form high concentration source/drain layers of the reverse conductive type;

doping impurities of one conductive type into said layer of the reverse conductive type by ion implantation to form a body layer of one conductive type;

forming a first gate electrode for a first MOS transistor on a gate oxide film after the gate oxide film is formed on said substrate to form a second gate electrode for a second MOS transistor on said body layer of one conductive type, wherein the body layer is formed only under the gate electrode; and

forming source/drain layers of the reverse conductive type so that they are adjacent to said first gate electrode using a resist film coating an area except areas where the source/drain layers for said first MOS transistor are formed as a mask.--

--15. (Amended) A method of manufacturing a semiconductor device according to Claim 14, further comprising [a step of] doping an impurity for forming a reverse conduction type layer by ion implantation.--

--16. (Amended) A method of manufacturing a semiconductor device according to Claim 7, wherein [said step of] doping impurities of one conductive type into said semiconductor layer to form a body layer comprises [a step of] doping by ion implantation.--

--17. (Amended) A method of manufacturing a semiconductor device according to Claim 10, wherein [said step of] doping impurities of one conductive type into said semiconductor layer to form a body layer comprises [a step of] doping by ion implantation.--

--18. (Amended) A method of manufacturing a semiconductor device according to Claim 12, wherein [said step of] doping impurities of one conductive type into said semiconductor layer to form a body layer comprises [a step of] doping by ion implantation.--

--19. (Amended) A method of manufacturing a semiconductor device according to Claim 14, wherein [said step of] doping impurities of one conductive type into said semiconductor layer to form a body layer comprises [a step of] doping by ion implantation.--

--22. (Amended) A method of manufacturing a semiconductor device comprising:

forming source/drain regions of a second conductive type in a semiconductor of a first conductive type [~~and a semiconductor layer of a first conductive type constituting a channel located between the source/drain regions of the second conductive type, the method comprising:~~];

doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form [the] a semiconductor layer of the first conductive type comprising a channel located between the source/drain regions; and

doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer.--

--23. (Amended) A method of manufacturing a semiconductor device comprising:

forming low concentration source/drain regions of a second conductive type in a semiconductor of a first conductive type[,];

forming high concentration source/drain regions of the second conductive type in the low concentration source/drain regions [and a semiconductor layer of the first conductive type constituting a channel located between the source/drain regions of the second conductive type, the method comprising:];

doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form the semiconductor layer of the first conductive type comprising a channel located between the source/drain regions; and

doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer.--

--24. (Amended) A method of manufacturing a semiconductor device comprising:

doping impurities of a second conductive type into a semiconductor of a first conductive type to form low concentration source/drain regions of the second conductive type;

doping impurities of the second conductive type into the semiconductor of the first conductive type to form high concentration source/drain regions of the second conductive type in the low concentration source/drain regions, wherein the low concentration source/drain regions surround the high concentration source/drain regions;

doping impurities of the first conductive type into the semiconductor of the first conductive type to form a semiconductor layer of the first conductive type constituting a channel located between the source/drain regions of the second conductive type;

doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer; and

forming a gate electrode on a gate oxide film provided on the semiconductor of the first conductive type, wherein the low concentration source/drain regions extends from under the gate electrode.--

--27. (Amended) A method of manufacturing a semiconductor device comprising:

forming a first transistor having high resistance to voltage and a second transistor having high resistance to voltage both having low concentration source/drain regions of a second conductive type in a semiconductor of a first conductive type[,];

forming high concentration source/drain regions of the second conductive type in the low concentration source/drain regions and a gate electrode formed on a gate oxide film provided on the semiconductor, wherein the low concentration source/drain regions extend from under the gate electrode, and the low concentration source/drain regions surround the high concentration source/drain regions;[, the method comprising:]

doping impurities of the second conductive type by ion implantation, to form a second conductive type layer [continuing] continuous with the low source/drain regions of the second transistor having high resistance to voltage[,]; and

doping impurities of the first conductive type to form a body layer of the first conductive type below the gate electrode of the second transistor having high resistance to voltage, wherein the body layer parts the second conductive layer.--

--28. (Amended) A method of manufacturing a semiconductor device comprising:

[having] forming a first transistor having high resistance to and a second transistor having high resistance to voltage[, the method comprising:];

doping impurities of a second conductive type into a semiconductor of a first conductive type to form first low concentration source/drain regions of the second conductive type for the first transistor and second low concentration source/drain regions of the second conductive type for the second transistor;

doping impurities of the second conductive type into the first and second source/drain regions of the second conductive type to form first high concentration source/drain regions of the second conductive type for the first transistor and second high concentration source/drain regions of the second conductive type for the second transistor;

doping impurities of the second conductive type by using a resist film, as a mask, having an opening in a region for forming the second transistor to form a low concentration second conductive type layer connecting the second low concentration source/drain regions; and

doping impurities of the first conductive type by using a resist film, as a mask, having an opening at a part of the second conductive type layer to form a semiconductor layer of the first conductive type below a gate electrode of the second transistor, wherein the semiconductor layer of the first conductive type parts the low concentration second conductive type layer, and the low concentration source/drain regions extend from under the gate electrode, and the low concentration source/drain regions surround the high concentration source/drain regions.--